CHE-MING, CHANG

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EDUCATION

Ph.D. student in Electrical and Computer Engineering, University of Southern California
Overall GPA: **4.00 / 4.00** 08/2025 - Expected 05/2030
Research Topic: AI/ML for EDA and heterogeneous integration

B.S. in Electrical Engineering, National Taiwan University
Overall GPA: **4.17 / 4.30** 09/2020 - 06/2024
Dean's List Award 2023 Spring
TSMC Semiconductor Advanced IC Design Program

Highlighted Coursework: Logic Synthesis and Verification, Physical Design for Nanometer ICs, Integrated Circuit Design, Computer-aided VLSI System Design, Digital Signal Processing in VLSI, Machine Learning

SKILLS

Programming	C/C++, Python, Verilog, Tcl, Bash
EDA Tools	Synopsys VCS / Design Compiler / PrimeTime / Library Compiler, Cadence Innovus
Languages	Mandarin (Native), English (Proficient)

PUBLICATION

[1] **Che-Ming Chang**, Rongjian Liang, Haoyu Yang, Pin-Han Chen and Sung Kyu Lim, "RouteFormer: Learning-Based Incremental Timing-Driven Global Routing," in *Proc. of ISPD*, Mar 2027.

[2] **Che-Ming Chang** and Sung Kyu Lim, "Physical Design Algorithms for Logic Folding and Fine-Grained Logic-on-Logic 3D ICs," in *Proc. of ASPDAC*, Jan 2027.

[3] **Che-Ming Chang**, Shao-Yu Lo, Yao-Wen Chang and Sung Kyu Lim, "Encoding Symmetries into Operator Learning: Towards Accurate Multi-Physics Simulation in Advanced Packaging," in *Proc. of ASPDAC*, Jan 2027.

[4] Pin-Han Chen, Chanhee Yang, Sungchul Joo, Hyungsoo Moon, **Che-Ming Chang**, Taek-Soo Kim and Sung Kyu Lim, "WAFER: Warpage Analysis via Fourier-Enhanced Residual Calibration for Large-Scale 2.5D IC Designs," in *Proc. of ICCAD*, November 2026, pp. 1-9.

[5] **Che-Ming Chang**, Prashanth Vijayaraghavan, Charles Mackin, Ashutosh Jadhav, Hsinyu Tsai, Vandana Mukherjee and Ehsan Degan, "CODMAS: A Dialectic Multi-Agent Collaborative Framework for Structured RTL Optimization," in *Proc. of EACL Industrial Track*, March 2026.

[6] Shao-Yu Lo, **Che-Ming Chang** and Yao-Wen Chang, "Advanced Packaging Warpage Modeling with DeepONet-Based Operator Learning," in *Proc. of ICCAD*, October 2025.

[7] **Che-Ming Chang**, Jie-Hong Roland Jiang, Dah-Wei Chiou, Ting Hsu and Guin-Dar Lin, "Quantum Circuit Compilation for Trapped-Ion Processors with the Drive-Through Architecture," in *IEEE Trans. Quantum Eng.*, vol. 6, pp. 1-14, 2025.

[8] Cheng-Yu Chiang, Yi-Hsien Chiang, Chao-Chi Lan, Yang Hsu, **Che-Ming Chang**, Shao-Chi Huang, Sheng-Hua Wang, Yao-Wen Chang and Hung-Ming Chen, "Mixed-Size Placement Prototyping Based on Reinforcement Learning with Semi-Concurrent Optimization," in *Proc. of ASPDAC*, January 2025, pp. 893–899.

RESEARCH EXPERIENCE

Southern California Computer-Aided Design (SCCAD) Lab 08/2025 - Present
Graduate Research Assistant, Advised by Prof. Sung Kyu Lim *Los Angeles, CA*

- Researched in ML-based global routing optimization.
- Researched in analytical floorplanning for 3D IC considering advanced packaging benefits.

Qualcomm, Methodology team 05/2026 - 08/2026
Research Intern, Advised by Mingyu Woo *San Diego, CA*

- Enhanced internal ECO-stage Vt assignment algorithm integrated with Synopsys PrimeTime.
- Delivered up to 26% flow runtime improvement, 36% TNS improvement during leakage power optimization on SoC-scale production designs.

Electronic Design Automation Lab 08/2023 - 01/2025
Research Assistant, Advised by Prof. Yao-Wen Chang *Taipei, Taiwan*

- Assisted in RL for concurrent macro placement project, demonstrated 12.3% / 9% additional HPWL reduction on ISPD'05 benchmarks compared to DREAMPlace / modern ML-based placer GraphPlanner.
- Developed an operator learning framework to predict warpage in advanced packaging designs, achieving 435× speedup over 8-core finite element method while maintaining an average error of 1.9%.

IBM Almaden Research Center, AI for EDA group 06/2024 - 09/2024
Research Intern, Advised by Prashanth Vijayaraghavan *San Jose, CA*

- Developed a multi-agent framework for HDL code optimization by retrieving domain-specific knowledge into the code generation process, aided with compiler and simulator feedback.
- Achieved 20% / 10% improvements for larger LLMs /small fine-tuned LLMs compared to zero-shot and ReAct / Chain-of-Thought baseline on HDL optimization tasks.

Applied Logic and Computation in System Design Lab 09/2022 - 06/2024
Research Assistant, Advised by Prof. Jie-Hong Roland Jiang *Taipei, Taiwan*

- Proposed an analytical method to compile a QASM circuit onto a "drive-through" modular architecture by gate partitioning followed by a fidelity-aware placement.
- Achieved 10.8% / 9.6% higher fidelity compared to modern qubit mappers SABRE / t|ket⟩.

PROJECT EXPERIENCE

Approximate Logic Synthesis with Multi-Objective Simulated Annealing 10/2023 - 12/2023
Final Project in Logic Synthesis and Verification, GitHub *Taipei, Taiwan*

- Utilized multi-objective simulated annealing to synthesize approximate circuits within the given error bound based on the synthesis tool ABC.
- Demonstrated substantial area reduction (8-98%) over IWLS benchmarks within 1% error rate and shows quality (5-91%) and runtime improvements over the existing ALS tool ALSRAC.

AWARDS AND HONORS

ICCAD Student Scholar Program Grant, ICCAD 10/2025
Taiwan Chip-based Industrial Innovation Program Research Scholarship, NSTC 09/2024 - 01/2025
Scholarship for Overseas Internship Program, NTU / Ministry of Education 06/2024 - 08/2024
Research Scholarship, MediaTek-NTU Research Center 03/2024- 06/2024
Second Prize and Global Nominee, NASA Space App Challange 10/2023
College Student Research Scholarship, NSTC 08/2023 - 02/2024

PROFESSIONAL SERVICE

Reviewer for 45th International Conference on Computer-Aided Design (ICCAD'26)
Reviewer for 34th International Symposium on Physical Design (ISPD'25)
Volunteer for 27th International Conference on Quantum Information Processing (QIP'24)
Volunteer for the First IEEE International Workshop on LLM-Aided Design (LAD'24)